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(54) SEMICONDUCTOR DEVICE AND PRODUCTION METHOD THEREFOR

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a structure and a production method for semiconductor device, with which a dedicated process is not added as conventional when forming a triple well structure for preventing the malfunction of a circuit caused by a wafer noise current.

SOLUTION: N+ type embedded layers (6A and 6B) are formed while being superimposed on an N-type well area 2B and the bottom of an N-type collector layer 4 by the same process. The N+ type embedded layer 6B has an effect to reduce the resistance of the collector layer 4 of a bipolar transistor. Besides, the N+ type embedded layer 6A is integrated with the N-type well area 2B and deep N-type well areas (2B and 6A) are formed.

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CLAIMS

[Claim(s)]

[Claim 1] the 2nd conductivity type formed on the semi-conductor substrate of the 1st

conductivity type -- a well -- a field and this 2nd conductivity type -- a well -- the 1st conductivity type formed in the front face in a field -- a well -- with a field this 1st conductivity type -- a well -- with the MOS transistor of the 2nd electric conduction channel mold formed in the field In the semiconductor device equipped with the 2nd conductivity-type collector layer formed on said semi-conductor substrate, the 1st conductivity-type base layer formed in the front face of this 2nd conductivity-type collector layer, and the 2nd conductivity-type emitter layer formed in this 1st conductivity-type base layer said 2nd conductivity type -- a well -- the semiconductor device characterized by superimposing on the pars basilaris ossis occipitalis of a field and said 2nd conductivity-type collector layer, and forming the embedding layer (6A, 6B) of the 2nd conductivity type at the same process.

[Claim 2] said 2nd conductivity type -- a well -- the semiconductor device indicated to claim 1 characterized by forming the field and said 2nd conductivity-type collector layer at the same process.

[Claim 3] said 1st conductivity type -- a well -- the semiconductor device indicated to claim 1 characterized by forming the field and the 1st conductivity-type base layer at the same process.

[Claim 4] the embedding layer of said 2nd conductivity type -- said 2nd conductivity type -- a well -- the semiconductor device indicated to claim 1 characterized by including a high-concentration impurity as compared with a field and said 2nd conductivity-type collector layer.

[Claim 5] the semi-conductor substrate top of the 1st conductivity type -- the 2nd conductivity type -- a well -- the process which forms a field and the 2nd conductivity-type collector layer -- said 2nd conductivity type -- a well -- the front face in a field -- the 1st conductivity type -- a well -- the process which forms the 1st conductivity-type base layer in the front face of said 2nd conductivity-type collector layer while forming a field -- It superimposes on the pars basilaris ossis occipitalis of a field and said 2nd conductivity-type collector layer. said 2nd conductivity type -- a well -- the process which forms the embedding layer (6A, 6B) of the 2nd conductivity type, and said 1st conductivity type -- a well -- the process which forms a gate electrode in a field -- said 1st conductivity type -- a well -- the manufacture approach of the semiconductor device characterized by both having the process which forms the 2nd conductivity-type source field and a drain field in a field, and which forms the 2nd conductivity-type emitter layer in said 1st conductivity-type base layer.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the semiconductor device which integrated the MOS transistor and the bipolar transistor on the same semi-conductor substrate, and its manufacture approach.

[0002]

[Description of the Prior Art] in recent years, the system LSI which included DRAM and the flash memory in Logic LSI, and formed them into 1 chip and which was carried out is developed. A big substrate current occurs in the circuit which carries out dynamic actuation of DRAM (Dynamic Random Access Memory) etc. This substrate current flowed into the logic LSI field, and had caused malfunction of a logical circuit. in order [then,] to solve this problem -- triple one -- a well -- structure was proposed.

[0003] drawing 5 -- triple one -- a well -- it is the sectional view showing the CMOS semiconductor device which adopted structure. the DRAM field on the semi-conductor substrate 101 -- the 1st N -- a well -- a field 102 and P -- a well -- a field 103 adjoins and is formed. N well, bias of the field 102 is carried out by supply voltage Vdd, and, on the other hand, the field 103 is grounded P well. the 1st N -- a well -- a field 102 -- a P channel mold MOS transistor and P -- a well -- an N channel mold MOS transistor is formed in a field 103 (un-illustrating).

[0004] a logical-circuit field -- the 1st N -- a well -- the 2nd well deeper than a field 103 -- the field 104 is formed. the 2nd well -- the inside of a field 104 -- further -- P -- a well -- the field 105 is formed. moreover, the 2nd well -- bias of the field 104 is carried out with supply voltage Vdd -- having -- **** -- on the other hand -- P -- a well -- the field 105 is grounded. An N channel mold MOS transistor is formed in a field 105 P well (un-illustrating). moreover, the 2nd well -- a field 104 -- adjoining -- N -- a well -- the

field 106 is formed. this N -- a well -- a P channel mold MOS transistor is formed in a field 106 (un-illustrating).

[0005] according to the configuration of the CMOS semiconductor device mentioned above -- a logical-circuit field -- setting -- the 2nd well -- the inside of a field 104 -- P -- a well -- the field 105 is formed. here -- the 2nd well -- a field 104 and P -- a well -- the substrate noise current In generated in the DRAM field since reverse bias of the field 105 was carried out -- the semi-conductor substrate 101 and the 2nd well -- the potential barrier of the PN junction which consists of fields 104, and the 2nd well -- a field 104 and P -- a well -- the potential barrier of the PN junction which consists of fields 105 -- P -- a well -- flowing in a field 105 is prevented.

[0006] moreover, the 2nd well -- since the field 104 is formed deeply, it is prevented that the substrate noise current In flows into a logical-circuit field by existence of this PN-junction barrier.

[0007] By these, since the inflow of the substrate current In is prevented by field 105 grade P well, malfunction of a logical circuit can be prevented.

[0008]

[Problem(s) to be Solved by the Invention] triple one mentioned above -- a well -- according to structure, actuation of a logical circuit can be stabilized except for the effect of the substrate noise current In generated in circuit fields which carry out dynamic operation, such as DRAM.

[0009] however, the 2nd conventionally deep well -- since the exclusive process for forming a field 104 was carried out -- the usual twin -- a well -- there was a problem that a production process will increase as compared with structure.

[0010]

[Means for Solving the Problem] the 2nd conductivity type which it succeeded in order that this invention might solve the above-mentioned technical problem, and was formed on the semi-conductor substrate of the 1st conductivity type -- a well -- with a field this 2nd conductivity type -- a well -- the 1st conductivity type formed in the front face in a field -- a well -- with a field this 1st conductivity type -- a well -- with the MOS transistor of the 2nd electric conduction channel mold formed in the field In the semiconductor device equipped with the 2nd conductivity-type collector layer formed on said semi-conductor substrate, the 1st conductivity-type base layer formed in the front face of this 2nd conductivity-type collector layer, and the 2nd conductivity-type emitter layer formed in this 1st conductivity-type base layer said 2nd conductivity type -- a well -- it is characterized by superimposing on the pars basilaris ossis occipitalis of a field and said 2nd conductivity-type collector layer, and forming the embedding layer

(6A, 6B) of the 2nd conductivity type at the same process.

[0011] Generally, in the semiconductor device which integrated the MOS transistor and the bipolar transistor of a vertical mold, the embedding layer (6B) of the 2nd conductivity type for lowering the collector resistance of the bipolar transistor of a vertical mold is formed.

[0012] then, an invention-in-this-application person -- the formation location of the embedding layer (6B) of the 2nd conductivity type -- paying one's attention -- the 2nd conductivity type -- a well -- it superimposes on the pars basilaris ossis occipitalis of a field and the 2nd conductivity-type collector layer, and the embedding layer (6A, 6B) of the 2nd conductivity type was formed at the same process. the 2nd deep conductivity type united with the embedding layer (6A) of the 2nd conductivity type by this, without completely increasing the production process of this kind of semiconductor device -- a well -- a field is formed.

[0013]

[Embodiment of the Invention] Next, it explains, referring to the semiconductor device concerning the gestalt of operation of this invention and its manufacture approach ******, drawing 1 , or drawing 4 . In addition, in drawing 1 thru/or drawing 4 , a logical-circuit formation field is shown in the right-hand side of a drawing, and the DRAM formation field is shown in left-hand side.

[0014] it is shown in drawing 1 -- as -- the P type silicon substrate 1 top -- N type -- a well -- field 2A, 2B, 2C, and the N type collector layer 4 are formed in coincidence. The ion implantation of at this time, for example, Lynn, is carried out on condition that 1x1013/cm2 of doses. Then, thermal diffusion of Lynn is carried out at 1100-degree about C temperature for several hours. The diffusion depth has desirable 1-2um.

[0015] moreover, silicon substrate 1 front face of a DRAM field -- P -- well 3A and N type -- a well -- the front face of field 2B -- P -- a well -- the P type base layer 5 is formed in the front face of field 3B and the N type collector layer 4 at coincidence. The ion implantation of at this time, for example, the boron, is carried out on condition that 1x1013/cm2 of doses. Then, thermal diffusion of the boron is carried out. the diffusion depth -- N type -- a well -- it is conditions that it is shallower than the diffusion depth of a field 2 and the N type collector layer 4.

[0016] Next, as shown in drawing 2 , a field oxidation process is performed by the selective oxidation method (Selective Oxi dation). thereby -- each -- a well -- the field oxide 6 for carrying out insulating separation of the between electrically is formed.

[0017] Next, as shown in drawing 3 , N+ mold embedding layer (6A, 6B) is formed. This process is a process of this invention by which it is characterized most. The

photoresist layer 7 is applied to the whole surface, and exposure and a development are performed using a predetermined photo mask. thereby -- N type -- a well -- opening is prepared in the field corresponding to field 2B and the N type collector layer 4. And N+ mold embedding layer (6A, 6B) is formed by carrying out the ion implantation of Lynn on condition that predetermined.

[0018] this time -- N type -- a well -- choosing acceleration energy suitably according to the diffusion depth of field 2B and the N type collector layer 4 -- the embedding layer (6A, 6B) of N+ mold -- N type -- a well -- it is superimposed and formed in the pars basilaris ossis occipitalis of field 2B and the N type collector layer 4. for example, N type -- a well -- as for the diffusion depth of field 2B and the N type collector layer 4, in the case of 2um extent, the acceleration energy of 2MeV extent is needed. What is necessary is just to use thermal diffusion together on the engine performance of ion implantation equipment, when high acceleration energy is unrealizable. moreover -- although the dose of an ion implantation can be chosen suitably -- the reduction in resistance, and a deep well -- for formation, it is desirable to consider as an about two 1x1014-/cm high-dose amount.

[0019] Here, N+ mold embedding layer 6B is effective in lowering resistance of the collector layer 4 of a bipolar transistor. moreover, embedding layer 6A of N+ mold -- N type -- a well -- it unites with field 2B -- having -- deep N type -- a well -- a field is formed.

[0020] Next, as shown in drawing 4 , various kinds of transistors are formed. first, gate dielectric film -- minding -- the gate electrode G -- N type -- a well -- a field (2A, 2C) and P type -- a well -- it forms in a field (3A, 3B). Next, the ion implantation of arsenic is performed using a predetermined mask, and the source layer and drain layer of N+ mold are formed. It can come, simultaneously N+ mold collector layer and N+ mold emitter layer are formed.

[0021] Thereby, an N channel mold MOS transistor (9 10) and the NPN mold bipolar transistor 12 are formed. Next, ion implantations, such as boron and BF2, are performed using a predetermined mask, and the source layer and drain layer of P+ mold are formed. Thereby, a P channel mold MOS transistor (8 11) is formed.

[0022] here -- a silicon substrate 1 -- touch-down (0V) -- carrying out -- N -- a well -- bias of the field (2A, 2B, 2C) is carried out to supply voltage Vdd (for example, 5V). Moreover, a field (3A, 3B) is grounded P well. Then, the reverse bias of field 2B, and N+ mold embedding layer 6A and a silicon substrate 1 is carried out N well. Moreover, the reverse bias of the field 2B is carried out to field 3B N well P well. By preparing these PN junctions by which the reverse bias was carried out, it is prevented that the

substrate noise current In generated in the DRAM field flows in field 3B P well. Moreover, since it unites with N+ mold embedding layer 6A and field 2B is formed deeply N well, it is prevented that the substrate noise current In flows into a logical-circuit field.

[0023] according to this operation gestalt -- the same process as the formation process of N+ mold embedding layer 6B of the NPN mold bipolar transistor 12 -- N+ mold embedding layer 6A -- N type -- a well -- since it superimposes and forms in the pars basilaris ossis occipitalis of field 2B, without it adds an exclusive process -- deep N type -- a well -- a field (2B, 6A) can be formed.

[0024] moreover, N type -- a well -- since the field (2A, 2B, 2C) and the collector field 4 are formed at the same process, production processes are reduced. moreover, P type -- a well -- since the field (3A, 3B) and the P type base layer 5 are also formed at the same process, production processes are reduced.

[0025] furthermore, the high impurity concentration of N+ mold embedding layer (6A, 6B) -- N type -- a well -- considering as high concentration as compared with a field (2B) -- N type -- a well -- since it becomes easy to be spread more deeply from the pars basilaris ossis occipitalis of a field (2B), it can prevent easily that a substrate noise current flows into a logical-circuit field. Moreover, since it becomes easy to generate recombination with an electron even when a substrate noise current is a hole current, and it flows in this N+ mold embedding layer (6B), it is expected that the substrate noise current itself will be extinguished.

[0026]

[Effect of the Invention] triple one for preventing malfunction of the circuit resulting from a substrate noise current according to this invention, as explained above -- a well -- since it becomes unnecessary to add an exclusive process like before in forming structure, big effectiveness is done so to reduction of a manufacturing cost, and compaction of TAT.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is a sectional view for explaining the manufacture approach of the semiconductor device concerning the operation gestalt of this invention.

[Drawing 2] It is a sectional view for explaining the manufacture approach of the semiconductor device concerning the operation gestalt of this invention.

[Drawing 3] It is a sectional view for explaining the manufacture approach of the semiconductor device concerning the operation gestalt of this invention.

[Drawing 4] It is a sectional view for explaining the manufacture approach of the semiconductor device concerning the operation gestalt of this invention.

[Drawing 5] It is the sectional view showing the semiconductor device concerning the conventional example.